Amendments

In the Specification:

Please substitute paragraph [0005] with the following paragraph:

A1

A major consideration in a superscalar RISC processor is how to execute multiple instructions in parallel and out-of-order, without incurring data errors due to dependencies inherent in such execution. Data dependency checking, register renaming and instruction scheduling are integral aspects of the solution. A detailed discussion of storage conflicts, register renaming and dependency mechanisms is found in related U.S. Patent No. 5,497,499 to Garg *et al.* (hereinafter referred to as the '499 patent).

Please substitute paragraph [0053] with the following paragraph:

A2

MONDEP 808 determines which dependencies have disappeared by comparing the tags of retiring or recently-retired instructions with the lower three bits of the renamed sources of each instruction. Information regarding retired instructions is sent to MONDEP 808 via a bus 828 from a retirement unit (not shown; the details of a retirement unit that can be used to generate these signals is disclosed in related U.S. Patent No. 5,826,055 to Wang *et al.*). If there is a match, then MONDEP 808 knows that the dependency has been removed and the outputs of MONDEP 808 outputs which instructions' inputs have been moved from the temp buffer to the register file. These output signals are sent to RFMXING 806 and RDY_GEN 810 via buses 822.

In the Claims:

Please cancel claims 1-11 without prejudice or disclaimer.

Please add the following new claims 12-20: